CASCaded H-BRIDGE AsymmetricAL 11-LEVELS Optimization

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Abstract - The following dissertation has the aim to investigate this multilevel topology, starting from the basis. The modeling methodology for this converter which is harmonic elimination control will be analyzed. Thus the contribution of this paper can be summarized mainly by the fact that the pre-calculated PWM control used to control the symmetrical structure, as applied to the asymmetrical structure with a reduced number of cells, provides the same performance level resolution and signal strength to the load terminals. Thus guaranteeing a report voltage frequency constant, the same for the three cells. This allows us to use different drivers till MOSFET, IGBT and GTO, therefore we have for each cell a good performance from the intrinsic properties of each semiconductor.

Index terms – Cascaded H-bridge asymmetrical converters, harmonic elimination control, THD.

I. INTRODUCTION

Cascade multilevel inverter (CMLI) is more recent and popular type of power electronic converter that synthesizes a desired output voltage from several levels of dc voltages as inputs. If sufficient number of dc sources is used, a nearly sinusoidal voltage waveform can be synthesized. CMLI offers several advantages such as, its capabilities to operate at high voltage with lower dv/dt per switching, high efficiency and low electromagnetic interference [EMI]. CMLI is one of the most important topology in the family of multilevel and multi pulse inverters. It requires least number of components with compare to diode-clamped and flying capacitors type multilevel inverters and no specially designed transformer is needed as compared to multi pulse inverter. It has modular structure with simple switching strategy and occupies less space [1], [3].

A complete analysis for an 11-levels inverter using 5 H-bridges per phase then 3 H-bridges in series is presented. It is focused on a general design principle of a uniform step 11 levels converters; with K series-connected full bridges inverters per phase. A new design terminology is proposed and analytical relationships are established.

possible cell output levels are exploited. While there are Simulation results shown the reliability of the design approach suggested.

II. SURVEY OF CASCaded H-BRIDGE ASYMMETRICAL TOPOLOGIES

II.1. Cascaded H-bridge multi levels concept

To overcome the limitations linked to the maximum voltage blocking capability of existing power semiconductor devices and to provide a large number of output levels without increasing the number of converters, asymmetrical 11-levels converters (A11LC) can be used [3, 4]. The investigated topology is shown in fig.1 with 5 symmetrical cells [(a)] and 3 asymmetrical cells [(b)] cascaded H-bridge legs.

![Fig.1 Configuration of single-phase series H-bridges 11-levels generated by: a) 5 symmetrical cells - b) 3 asymmetrical cells](image-url)
no limitations on the level of diode-clamped or flying-capacitor inverter, which can be even or odd, cascaded H-bridge can have only odd numbers of levels; indeed the first cell gives three levels whereas the others always add two levels more. 

So Fig. 1 permits to put symmetrical versus asymmetrical multi levels converter (AMLC). 

As shown in Fig.1 (a) the SMLC is defined by the fact that all feeding partial DC-voltages sources (DCVS) are equivalent, have the same value and are series connected. In practice there are no such limits, and then the DCVS can be different. The DCVS are proposed at the maximum output voltage with the minimum number of cells and given switches. Choosing different input voltages [Fig.1 (b)] for each inverter allows obtaining the large cell and IGBT switches for the small one. This latter solution is known as AMLC. Choosing the same input voltage [Fig.1 (a)] for each inverter allows obtaining the maximum output voltage with the minimum number of cells and given switches. Choosing different input voltages [Fig.1 (b)] for each cell allows obtaining the maximum output resolution with the minimum number of cells. This distinction clearly shows two different fields of applications, high voltage inverters and high resolution inverters, which correspond respectively to symmetrical and asymmetrical multi levels inverters. Of course, if a higher resolution for a high voltage inverter is needed, it is possible to combine the two techniques.

II.2. Multi levels cascaded H-bridge asymmetrical inverter performance

Asymmetric multi levels converters (AMC) can optimize the number of output levels (any odd number from $2K+1$ to $3K$), by using H-bridges scaled in power of three, without increasing the number of converters. The corresponding “Asymmetrical” topology provides more flexibility to the designer. The shortcoming of this topology is that the H-bridges are not interchangeable and then, under certain faulty conditions, the converter cannot operate.

The AMC go one step ahead with DCVS varying in binary fashion, which gives an exponential increase in the number of levels. For ‘n’ such cascaded inverters, with DC voltage levels varying in binary fashion, $2n+1$ distinct voltage levels may be achieved. The DCVS supplying partial inverters are supposed to be rationally unbalanced.

AMC are a viable solution to increase the power with a relatively low stress on the components and with simple control systems. Moreover, they present several other advantages. First of all, they generate better output waveforms with a lower $dv/dt$ than the standard converters. Then, AMC increase the power quality due

crenels or impulses by alternation. Whether odd or even number, $C$ is represents also the number of angles of

to the great number of levels of the output voltage: in this way, the AC side filter can be reduced, decreasing its costs and losses. Furthermore, AMC can operate with a lower switching frequency than 2-level converters, so the electromagnetic emissions they generate are weaker, making less severe to comply with the standards. Furthermore AMC can be directly connected to high voltage sources without using transformers; this means a reduction of implementation and costs.

III. H-BRIDGE ASYMMETRICAL 11-LEVELS OPTIMIZATION

In general, the Fourier series expansion of the staircase output voltage waveform is as shown in Fig.2.

III.1 Harmonic elimination method

In applications where the voltage magnitude and the frequency are relatively fixed, we are not in need of a modulated voltage [4]. In this case, the fundamental wave is sufficient for the voltage generation whose harmonic rate of distortion is weak. The harmonic elimination method consists in quantifying this reference voltage, in a given number of steps [5]. This modulation technical will be used to control symmetric multilevel inverter with five series-connected H-bridges. It consists in forming the output wave of the inverter of a succession of crenels or impulses by alternation. Whether odd or even number, $C$ is represents also the number of angles of
overlap per quarter of period and determines the width of the whole of the crenels. The angles of overlap are given in such way to eliminate certain harmonics. In the present study we were interested to eliminate the first harmonics (5, 7, 11, and 13). The fig. 3 illustrates the waveforms and switching method of 11 levels cascade inverter.

\[ \theta_1 = 5.5510^\circ, \theta_2 = 16.3669^\circ, \theta_3 = 23.2811^\circ, \theta_4 = 38.2607^\circ, \theta_5 = 58.699^\circ. \]

The angles \( \theta_i \) (i = 1, 2, 3, 4, and 5) are used to start the switches, the control signals equivalent to these angles are shown in fig. 5.

III.2 Control Strategy

The five switching angles, \( \theta_i \) (i = 1, 2, 3, 4, and 5), are calculated offline to minimize the harmonics for each modulation index \( m_a \) in order to have a total output voltage with a harmonic minimal distortion rate. The correct solution to (5) means that the output voltage of the 11-levels inverter will not contain the 5th, 7th, 11th, and 13th harmonic components.

\[
\begin{align*}
\alpha(5\theta_1)+\alpha(5\theta_2)+\alpha(5\theta_3)+\alpha(5\theta_4)+\alpha(5\theta_5) &= 0 \\
\alpha(7\theta_1)+\alpha(7\theta_2)+\alpha(7\theta_3)+\alpha(7\theta_4)+\alpha(7\theta_5) &= 0 \\
\alpha(11\theta_1)+\alpha(11\theta_2)+\alpha(11\theta_3)+\alpha(11\theta_4)+\alpha(11\theta_5) &= 0 \\
\alpha(13\theta_1)+\alpha(13\theta_2)+\alpha(13\theta_3)+\alpha(13\theta_4)+\alpha(13\theta_5) &= 0
\end{align*}
\]

The evolution of conduction angles according to the modulation index \( m_a \) such as the depicted in fig. 4 are as follows:

For a better optimization of the waveform of the output voltage, for a modulation index \( m_a = 0.9 \), the conduction angles is as follows:

\[ \theta_1 = 5.5510^\circ, \theta_2 = 16.3669^\circ, \theta_3 = 23.2811^\circ, \theta_4 = 38.2607^\circ, \theta_5 = 58.699^\circ. \]
This strategy of control based on the conduction angles choices which satisfy the condition of symmetry, allows us indeed to have the commutation frequency of the switches equal to the fundamental frequency one, which minimizes the commutation losses, but different cells don’t have the same conduction time. It thus results in an unbalance in the distribution of the conduction losses.

The output voltages in fig.6 are as follows:

As shown in fig.6 and fig.7, we note that:
- With a symmetrical supply we obtain an output voltage which has $2^5+1$ levels of output voltage peak to peak.
- The output voltage has a good harmonic distortion rate ($\text{THD}_v = 8.33\%$) with harmonics elimination (5, 7, 11, 13).

We note that:
- The DCVSs of each cell are chosen in such a way as to have a level run well determined of $V_{AN}$ 11 levels as shown at fig.9.
- For each cell we use identical switches having the same technical parameters, but different from switches of the 2 others cells. Indeed voltage caliber and size of switches...
IV. SIMULATION AND RESULTS

We use the same angles $\theta_i$ ($i = 1, 2, 3, 4, 5$) point out before. The signal control and the output voltage of each cell relative to the angles are logging at fig.10. So we note that:

- The total number of each cell commutations depends on the value of the voltage which feeds it, therefore of its position in the structure of the converter.
- More the supply voltage of a cell is grand with regard to the others less those switches commuted.

The output voltage and the THD are given by respectively fig.11 and fig.12.

The 3 series cells AMLC the DCVS respectively E, 2E, 4E represent a supplementary degree of liberty which consist and permit to generate output phase voltage $V_{AN}$ 11 levels having the same $\text{THD}_v = 8.33\%$ with a reduce cells number (3 cells).
Fig. 11 wave form voltage of asymmetrical multilevel inverter with three series-connected H-bridges by elimination harmonic method

Fig. 12 Harmonic rates of the output voltage

Table 1 shows the result before and after the optimization using the asymmetrical topology. This strategy obtains the same value of THDv (8.33%) using only 3 cells and 12 semiconductors.

Table 1: Asymmetrical 11-levels optimization

<table>
<thead>
<tr>
<th>Topology</th>
<th>Cells number</th>
<th>Semiconductors number</th>
<th>THDv</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symmetrical</td>
<td>5</td>
<td>20</td>
<td>8.33%</td>
</tr>
<tr>
<td>Asymmetrical</td>
<td>3</td>
<td>12</td>
<td>8.33%</td>
</tr>
</tbody>
</table>

CONCLUSION

This paper deals with asymmetrical multi levels inverters. A generalized design principle of an asymmetrical multi levels converter was presented. The investigated topology is based with $K$ series-connected full bridges inverters per phase. It consists of series connected cells with different input voltages.

A complete analysis for 11-levels inverter has been presented and it is shown that a significant amount of THD reduction can be attained if all possible solution sets are computed. It has been shown that there are many possibilities to feed the partial H-bridge inverters to enhance the number of output voltage levels, without increasing the number of power switches [1, 4]. The cascade H-bridge asymmetrical 11-levels optimization is based on the choosing of different input voltages for each cell. This allows obtaining the maximum output resolution with the minimum number of cells.

This distinction clearly shows two different fields of applications, high voltage inverters and high resolution inverters, which correspond respectively to symmetrical and asymmetrical multi levels inverters.

A new optimal switching control strategy for these latter inverters was proposed. This strategy obtains the optimal result in terms of harmonic rates of the output voltage and consequently in terms of switching losses.

REFERENCES


